REMARKS

Claims 14 and 38 were objected to as being unclear. It is believed that the above amendments overcome that objection and reconsideration is requested.

All claims were rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Michael *et al.* (EP 0886454A2) in view of Brant *et al.* (US Patent 5,805,787). That rejection is respectfully traversed and reconsideration is requested.

The present invention is directed to a router within an interconnection network. Such routers carry information units such as packets between nodes. As information units flow through the routers, they must be temporarily stored before being forwarded onto a next router or destination. The routers are designed for rapid flow of data streams.

Though not related to a router, Ben-Michael does disclose an ATM switch which, like a router, is concerned with the rapid flow of data streams. As with the present invention, it is preferred that the data buffers be closely integrated with the primary switch circuitry, and like with the present invention, Ben-Michael provides expanded memory space. Though primarily directed to storage of flow control credits, Ben-Michael does indicate at page 7, lines 41-42 that the FIFO may be used to store data packets rather than credits. In either case, in keeping with its application to rapid handling of data streams, the expanded memory is in the form of FIFO.

Brant *et al.* relates to a cache memory which is positioned between a host computer 10 and a disk storage system 25. Such uses of cache memory are well known. The advantage of a cache memory is that, with a typical memory access pattern that exhibits temporal and spatial locality, data that has been recently recovered from disk storage is likely to be accessed again in the near future. Such data is retained in the cache and subsequent accesses can be made directly to the cache without the need for an additional access to disk.

Since all data in a data stream must flow out of the switch in the same order in which it arrives, the simple FIFO memory architecture is well suited to the Ben-Michael application. One skilled in the art would see no need or advantage to the more complicated cache memory system of Brant *et al.* in a data streaming application like Ben-Michael. The cache system enables unordered access to data made available on a probability basis, with the primary static disk storage always being available if there is a miss in the cache. In Ben-Michael, there is no static storage and there is no need for unordered access. Thus, there is no suggestion of combining the references.

A router as claimed deals with the rapid flow of data streams similar to Ben-Michael. However, unlike the ATM switch of Ben-Michael where virtual circuits through multiple nodes are pre-established so that data can flow generally uninterrupted, routers must arbitrate between data flows. While a data stream entering the Ben-Michael switch is guaranteed its output port, two data streams received at different input ports on a router may compete for the same output port. The router must arbitrate and block one data stream as the other flows through. The present inventors have recognized that, although a FIFO would be adequate for the guaranteed flow of a single data stream, it is not appropriate where data flow may be blocked so that different data streams may be retained in the buffer space for different periods of time. In the present invention, the rapidly accessible buffers and second set of more slowly accessed buffers perform not as a FIFO as in Ben-Michael, but as a cache system with information units evicted to the second set of buffers in accordance with an algorithm other than the order of receipt in the first buffer.

As discussed in the Manual of Patent Examining Procedure Section 706.02(j), "there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings." In the present case, there is no suggestion in Ben-Michael of using anything other than a FIFO memory architecture, and there is no suggestion in Brant *et al.* that a conventional cache memory positioned between a host processor and disk storage space might somehow be applied to buffer space for data streaming through the ATM switch of Ben-Michael.

Further, since Ben-Michael is an ATM switch and not a router which requires arbitration, even the non-obvious problem and solution recognized by Applicants would not apply to the ATM switch of Ben-Michael. Thus, it is respectfully submitted that all claims should be allowed.

With respect to claims 3, 18, 33 and 41 which recite virtual channels, the Examiner has referred to the virtual circuits of Ben-Michael and then refers to virtual channels, apparently using the two terms interchangeably. In fact, the two terms are very distinct. A virtual circuit in an ATM network is a path which is pre-established through multiple switch nodes for the flow of a data stream. A virtual channel, on the other hand, refers to buffer space which is required on a router to handle multiple data streams vying for a common destination port. In an ATM switch, data streams do not vie for an output port since the output port has been pre-assigned to a virtual circuit through which the data stream is flowing. This distinction between virtual channels, which must arbitrate for an output port, and a virtual circuit is a key to the cache memory solution of the present invention as compared to the appropriate FIFO solution in the ATM switch environment. Virtual channels and the problem of allocating buffer space for the virtual channels do not exist in an ATM switch. Accordingly, claims 3, 18, 33 and 41 should be allowed. Similarly, claims 7, 22 and 46-49 should be allowed.

With respect to claims 4, 19, 34 and 42, the Examiner has referred to the multiple FIFO pointers of multiple banks of Ben-Michael for a pointer array of pointers. The head and tail pointers of FIFOs would not be associated with individual channels as now recited in the claims.

With respect to claims 8, 10, 23, 25, 36-37 and 44, the Examiner has referred to the flow control of Ben-Michael and has concluded that a source would hold its data while the data packets are off loaded to the off chip memory. However, Ben-Michael teaches at page 5, lines 35-40 that delays in access to the off chip local memory can be tolerated because the middle portion of the FIFO does not require rapid access. Thus, Ben-Michael teaches that there would be no need to stop the arrival of new information units as recited in claims 8-10, 23-25, 36, 37 and 44. Accordingly, it is respectfully submitted that those claims are not suggested by Ben-Michael.

With respect to claims 13 and 28, it is respectfully submitted that Ben-Michael teaches neither a router nor a multicomputer interconnection network. Rather, Ben-Michael merely teaches a switch in an ATM network.

With respect to claims 14, 15, 30, 38, 39 and 45, a fabric router is one of many routers within a larger switch or router. Again, Ben-Michael only teaches ATM switches and those switches do not comprise fabrics of routers.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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